



Docket No.: 63979-029

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of	:	Customer Number: 20277
	:	
Takeshi TAKAGI	:	Confirmation Number:
	:	
Serial No.: 10/626,642	:	Group Art Unit:
	:	
Filed: July 25, 2003	:	Examiner: Unknown
	:	
For: SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING THE SAME		

**INFORMATION DISCLOSURE STATEMENT**

Honorable Commissioner for Patents and Trademarks  
Washington, D. C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

References listed on attached Form 1449 but not on the International Search Report are discussed in the specification.

A copy of the foreign search report is attached for the Examiner's information. Please note this is a PCT application in the entry of the National Phase in the U.S. and copies of the references cited were transmitted by WIPO and are believed to be in the file of the above identified application and readily available to the Examiner. However, to ensure that these references are available to the Examiner, we are providing copies of these

**Serial No.: 10/626,642**

references herewith. Since the Search Report was from the U.S. JPO or EPO search authorities, copies of these references should have been supplied to the USPTO under the trilateral agreement and are believed to be in the file of the above identified application and readily available to the Examiner. Therefore it is believed that Applicants have met all requirements regarding duty of disclosure under 37 CFR 1.56. Acknowledgement and consideration of these documents are respectfully requested.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Michael E. Fogarty  
Registration No. 36,139

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
(202) 756-8000 MEF:tlb  
Facsimile: (202) 756-8087  
**Date: February 20, 2004**



SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (PTO-1449)				ATTY. DOCKET NO. <b>63979-029</b>	SERIAL NO. <b>10/626,642</b>		
				APPLICANT <b>Takeshi TAKAGI</b>			
				FILING DATE <b>July 25, 2003</b>	GROUP		
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 5,512,771	04/30/1996	Hiroki et al.			
		US 2002/0005581 A1	01/17/2002	Kurata			
		US					
		US					
		US					
		US					
		US					
		US					
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
		JP 62-045071	02/27/1987	NEC CORP		(Japan w/English Abstract)	
		JP P2001-119026A	04/27/2001	SAMSUNG ELECTRONICS CO LTD		(Japan w/English Abstract)	
		JP 9-45903	02/14/1997	MATSUSHITA ELECTRIC IND CO LTD		(Japan w/English Abstract)	
		JP 3-69166	03/25/1991	NIPPON SOKEN INC		(Japan w/English Abstract)	
		JP 6-267972	09/22/1994	NEW JAPAN RADIO CO LTD		(Japan w/English Abstract)	
		JP P2002-100768A	04/05/2002	FUJITSU LTD		(Japan w/English Abstract)	
		JP 9-148564	06/06/1997	NEC CORP		(Japan w/English Abstract)	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		Wen-Chin LEE, et al., "Investigation of Poly-Si-xGe for Dual-Gate CMOS Technology", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998					
		T. GHANI, et al., "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", 1999 IEEE pp. 415-418					
		T. SKOTNICKI, et al., "Well-Controlled, Selectively Under-Etched Si/SiGe Gates for RF and High Performance CMOS", 2000 IEEE					
EXAMINER		DATE CONSIDERED					

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.